

Modeling Tools for Power Supply Impedance Analysis

Abstract

Impedance matching is an important aspect of power supply design. With a marginal design, unexpected input ripple will occur. This will add to output ripple and disturb other systems on the distribution network. In extreme cases, damage to the power supply or other equipment can occur. This paper intends to raise awareness of this issue and to provide analysis methods to evaluate specific systems.

Through a combination of mathematical demonstrations, SPICE modeling, and real-world testing, this presentation will explore how to ensure proper impedance matching in power converter systems. Key topics include proving the need for load impedance to exceed source impedance and exploring the concept of negative impedance in power converters. Modeling of current mode control and real-time division within SPICE is provided.

Additionally, this paper integrates SPICE models for controllers, EMI filters, and measurement networks, along with design equations and simulation results. Techniques for optimizing transient performance covered.

Notices

COPYRIGHT NOTICE

Published by Vito D'Erasmus, Copyright © 2024.

Unauthorized copying, in part or in whole, is prohibited without proper citation and referencing.

Created by V. D'Erasmus

Disclaimer of Liability

The information, observations, and conclusions provided in this document are offered as a free informational resource. All materials and information are provided "AS IS" and do not constitute professional or legal advice. No representation or warranty of any kind, express or implied, is made regarding the accuracy, adequacy, validity, reliability, availability, or completeness of the information contained in this document. Users should not use this information without independent verification and assume all risks associated with its use. Under no circumstances shall any liability be incurred for any loss or damage resulting from the use of or reliance on the information provided herein. Use of this document and reliance on its contents is solely at the user's own risk.

Modeling Tools for Power Supply Impedance Analysis

Table of Contents

1	Introduction	1
1.1	The Importance of Impedance Matching in Power Systems	1
1.2	Negative Characteristics in Power Supply Input Impedance	2
2	Average Model for Voltage Mode Impedance Analysis	4
2.1	Power Train SPICE Average Representation	4
2.2	Testing the Power Train	5
2.3	Closing the Voltage Mode Loop	6
2.4	Matching the EMI Filter	9
2.5	Impedance Margin for the VM Converter	10
3	Average Model for Current Mode Impedance Analysis	11
3.1	Mathematical Representation of Duty Cycle Generator	11
3.2	Emulating Division in PSPICE	12
3.3	Implementing the CMC Average Duty Cycle Generator	13
3.4	SPICE Representation of Average CMC Power Train	14
3.5	CMC Plant Gain	15
3.6	Control Loop and Compensation	16
3.7	Input Impedance Plot	18
3.8	CMC Input Impedance Plot	19
4	Effect of adding Line Impedance Stabilization Networks (LISN)	20
5	Effect of Using Transient Voltage Test Equipment	23

List of Equations

Equation 1-1: Gain Based on Impedance Ratio	1
Equation 2-1: Gain of the VM Plant	6
Equation 3-1: Average DC from Commanded Current	11

Modeling Tools for Power Supply Impedance Analysis

List of Figures

Figure 1-1: Source and Load Impedance	1
Figure 2-1: Power Train Spice Model	4
Figure 2-2: Power Train AC Analysis	5
Figure 2-3: VM Plant Gain and Phase based on Nodal Analysis	6
Figure 2-4: VM Compensator	7
Figure 2-5: VM Complete Loop	7
Figure 2-6: VM Compensator in SPICE	8
Figure 2-7: Total VM Loop Gain and Phase	8
Figure 2-8: EMI Filter Added to SPICE Model	9
Figure 2-9: VM Impedance Match Plot	9
Figure 2-10: VM Input Voltage Variation	10
Figure 3-1: VM Input Voltage Variation	11
Figure 3-2: Division Emulator	12
Figure 3-3: CMC Average Duty Cycle Generator	13
Figure 3-4: CMC Plant Average Model	14
Figure 3-5: CM Plant Gain and Phase	15
Figure 3-6: CMC with Voltage Controller	16
Figure 3-7: CMC Open Loop Response	17
Figure 3-8: CMC Impedance Match Margin Restored	19
Figure 4-1: Typical LISN from MIL-STD-461	20
Figure 4-2: LISN Impedance Curve	20
Figure 4-3: Impedance Match with LISN Connected	21
Figure 4-4: Impedance Margin Restored	22
Figure 5-1: Measured Output Impedance of Transient Power Source	23
Figure 5-2: Improved Transient Performance with Dampener	25
Figure 5-3: Transient Source Impedance with Dampener Added	25

1 Introduction

The importance of matching input EMI filters to power converters has been well-documented in prior publications, most notably in *MIL-HDBK-241 (Published by the DoD)*, *Advances In Switchmode Power Conversion* by Middlebrook and Cuk, and in *Fundamentals of Power Electronics* by Erickson and Maksimovic. This presentation builds on that foundational work by providing practical tools and simulation examples to enhance understanding. Additionally, it explores real-world scenarios, offering concrete solutions to the challenges encountered in designing and implementing matched impedance circuits.

1.1 The Importance of Impedance Matching in Power Systems

Whenever two electronic systems are connected, the source impedance and load impedance should be evaluated. This is demonstrated in Figure 1-1.

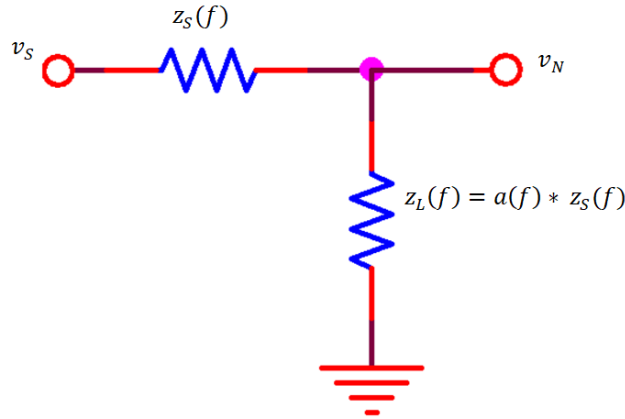


Figure 1-1: Source and Load Impedance

In this case, the Gain of the system $H(f)$ is the ratio of v_N to v_S . A simple nodal analysis yields the following.

$$H(f) = \frac{v_N}{v_S} = \frac{a(f)}{a(f) + 1}, \text{ where } a(f) = \frac{Z_L(f)}{Z_S(f)}$$

Equation 1-1: Gain Based on Impedance Ratio

In Equation 1-1, as $a(f)$ approaches -1, the gain theoretically becomes infinite. However, due to non-ideal component behavior, gain is constrained by large-signal limitations and the parasitic characteristics of components. Nevertheless, overlooking impedance matching can still result in unexpected and potentially unpredictable outcomes, highlighting the importance of careful design consideration.

1.2 Negative Characteristics in Power Supply Input Impedance

Switchmode power supplies are said to have a negative input impedance. Due to the high efficiencies achieved, the input power is relatively constant as a function of input line variations. Given that we can consider an example of a small signal sinewave riding on top of the input voltage to further analyze this effect.

Consider the following as input voltage.

$$v_{In}(t) = a \sin(\omega t) + V_{DC}$$

Keeping the input power constant, we can calculate input current as follows..

$$i_{In}(t) = \frac{P_{Const}}{a \sin(\omega t) + V_{DC}}$$

In absence of having an intuitive understanding of the equation above, we'll turn to a numerical example. But first note, in an extreme case where the AC component outweighs the DC component, the result will be a cosecant function. This would be a highly distorted sine wave, however the first harmonic would still be 180 degrees out of phase with the input.

For a more 'small signal' example, consider a 100W power supply with 28VDC nominal input with a 1V sine wave riding on the DC input.

The specific input current is calculated in the following figure.

Modeling Tools for Power Supply Impedance Analysis

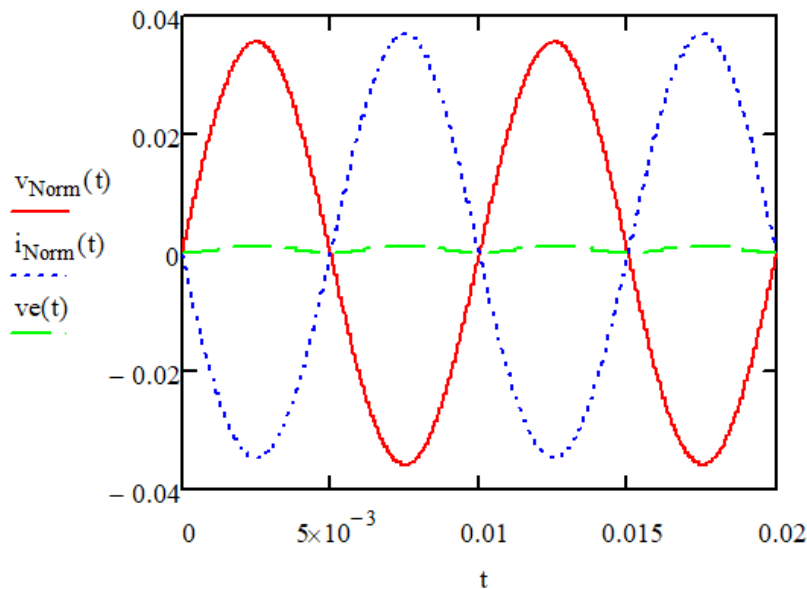
$$f_r = 100\text{Hz} \quad \omega = 2\pi \cdot f_r$$

$$a = 1\text{V} \quad V_{\text{DC}} = 28\text{V} \quad P = 100\text{W} \quad I_{\text{DC}} = \frac{P}{V_{\text{DC}}} = 3.571\text{A}$$

$$v_{\text{In}}(t) = a \cdot \sin(\omega \cdot t) + V_{\text{DC}} \quad i_{\text{In}}(t) = \frac{P}{v_{\text{In}}(t)}$$

$$v_{\text{Norm}}(t) = \frac{v_{\text{In}}(t)}{V_{\text{DC}}} - 1 \quad i_{\text{Norm}}(t) = \frac{i_{\text{In}}(t)}{I_{\text{DC}}} - 1$$

$$\text{Error} \quad v_e(t) = v_{\text{Norm}}(t) + i_{\text{Norm}}(t) \quad +$$



The input voltage and current are plotted above. The signals are normalized in amplitude and the DC components are removed.

The input voltage is a pure sine as this was a given at the start of this example. The input current appears to be a sine wave with 180 degree phase shift. Performing a Fourier Analysis shows that it is approximately 99% pure. The graph shows an error signal which is the addition of the two normalized signals. If the current was a pure sign wave, the error would not exist. We can see here that there is a second harmonic present. There are higher order harmonics present, but they are negligible.

2 Average Model for Voltage Mode Impedance Analysis

Average modeling is used here to focus on the frequency band of interest. A switching model may add value but the expense in complexity, simulation time and the time required to construct a converging model is not required to arrive at a successful design. Additionally, AC analysis tools built into the SPICE environment are not readily available when using a switching model. Using the tools in this way allows engineers to gain greater insight into the overall system stability.

2.1 Power Train SPICE Average Representation

The circuit in Figure 2-1 Shows an average voltage mode (VM) power train. Notice the use of parameters. Parameters are used so that values can be altered during sweeps to develop a family of curves. Node VF is the input voltage and node D is the duty cycle. D will later be generated by a control loop. Here, it is a constant 25% with a 0.01 VAC sine sweep applied to it. This VAC source is installed so that we can plot the 'Plant' gain for the VM converter.

Notice the presence of V6. This is currently set to zero, however we will later assign a value to this source to measure the input impedance.

The transformer is represented by E1 and G1. E1 transfers voltage to the secondary while G1 reflects current from the secondary to the primary. This is accomplished using parameters.

The phase parameter is provided so that multiple phase inverters could be represented. In general this should be the number of output inductors used in the specific buck derived topology.

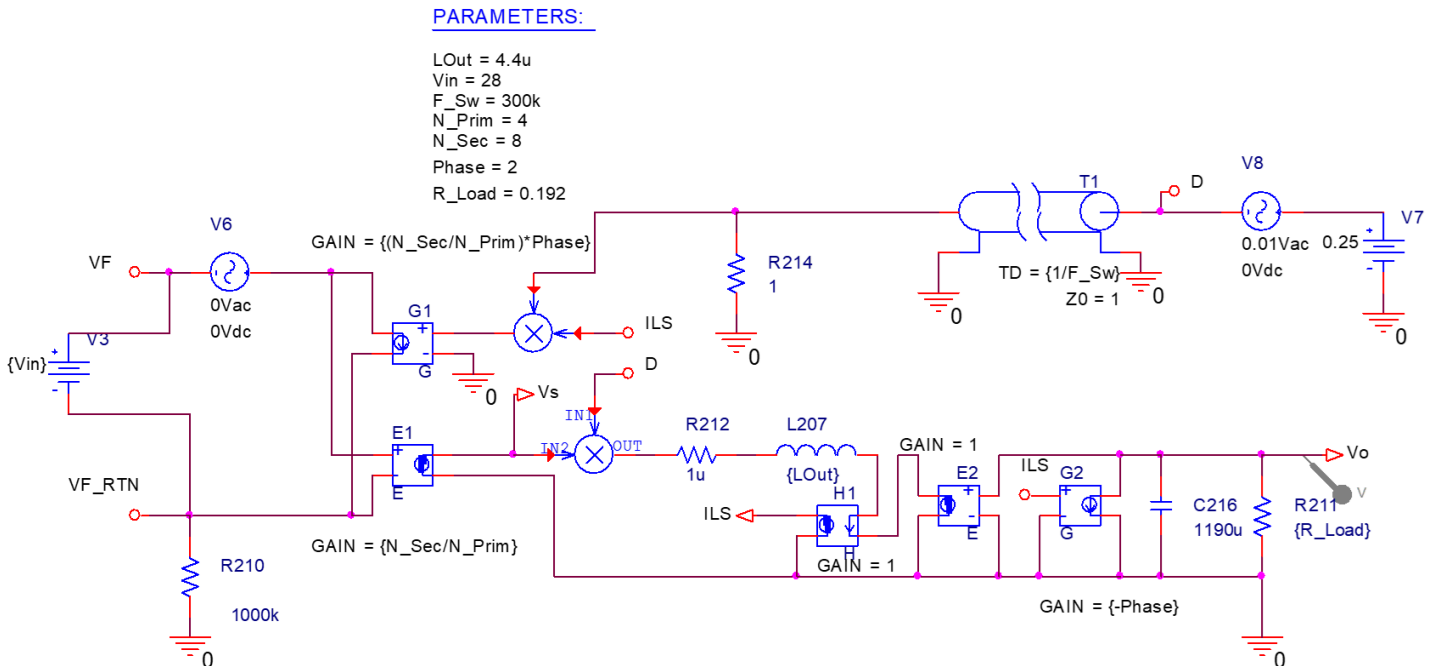


Figure 2-1: Power Train Spice Model

2.2 Testing the Power Train

An AC analysis is performed then the SPICE post-processing tool is used to plot the results. This tool allows for mathematical functions on the data, enabling direct production of plant gain and phase plots. While such plots can be created with a switching model, doing so requires significantly more skill, effort, and simulation time. The use of average models in AC analysis simplifies the process and enhances efficiency.

In the analysis, the use of parameters is demonstrated. The load is swept from 0.2 ohms to 0.8 ohms and the results are plotted as a family of curves.

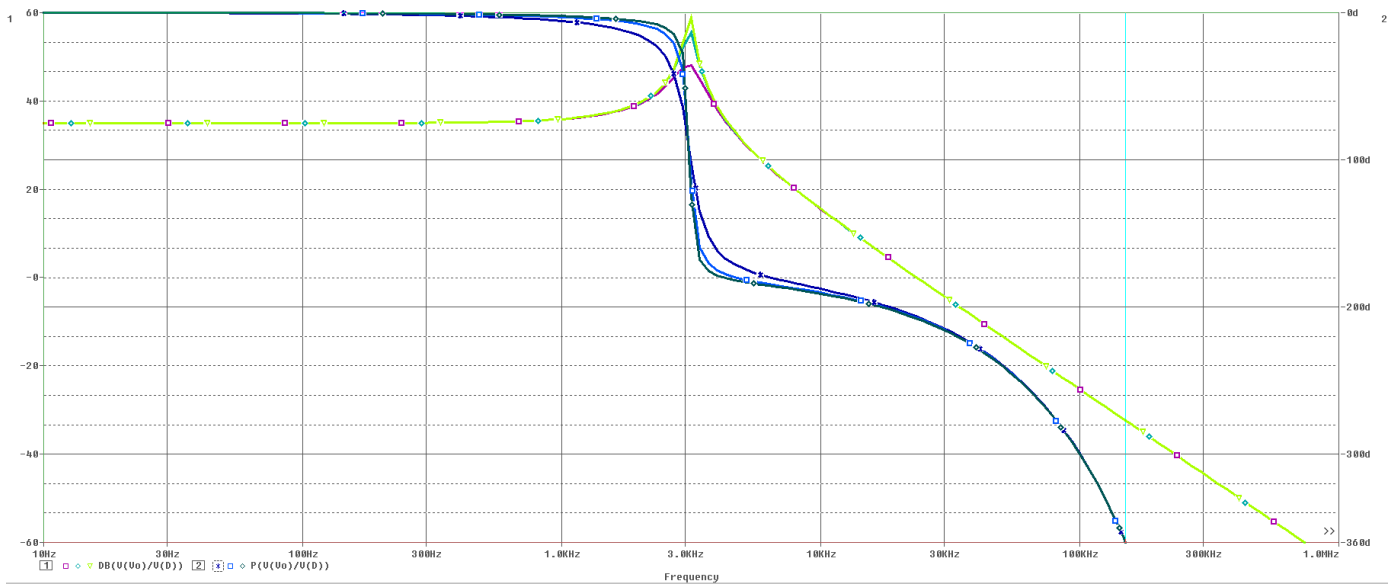


Figure 2-2: Power Train AC Analysis

It is interesting to note that, although one might expect the calculated break frequency to be around 2kHz based on the component values, the model places it at 3kHz. This discrepancy arises because the 'phase' parameter is set to 2 in this case, effectively halving the inductor value. As a result, SPICE correctly represents the break frequency. While SPICE does not explicitly divide the inductor value, the AC sweep inherently produces this effect.

2.3 Closing the Voltage Mode Loop

Closing control loops require patience and skill. Many difficulties arise when trying to construct a single function to compensate for a wide range of load, a range of capacitive load a range of input voltage, understanding the effects of parasitic contributors while trying to achieve some specified level of dynamic performance. A cook-book process can only go so far without knowing which of the previous variables will dominate the analysis.

Start by calculating the nominal DC gain of the VM plant, which is the target output voltage divided by the nominal duty cycle.

$$G_{DC} = Vin * \frac{n_s}{n_p}, \text{ where } n_s \text{ and } n_p \text{ are Primary and Secondary Turns}$$

For this example, we'll let the input voltage be a steady 28V, and n_s is 2 and n_p is 1. Therefore $G_{DC} = 56$.

Nodal analysis is used because it can be more interactive than the SPICE tool. The frequency dependent gain of the plant is calculated in Equation 2-1.

$$H_p(s) = G_{DC} \cdot \frac{s \cdot R_L \cdot R_{esr} \cdot Co + R_L}{s^2 \cdot \left(\frac{Lo}{Phase} \cdot Co \cdot R_L + \frac{Lo}{Phase} \cdot Co \cdot R_{esr} \right) + s \cdot \left(R_L \cdot R_{esr} \cdot Co + \frac{Lo}{Phase} \right) + R_L} \cdot e^{-s \cdot T_m}$$

Equation 2-1: Gain of the VM Plant

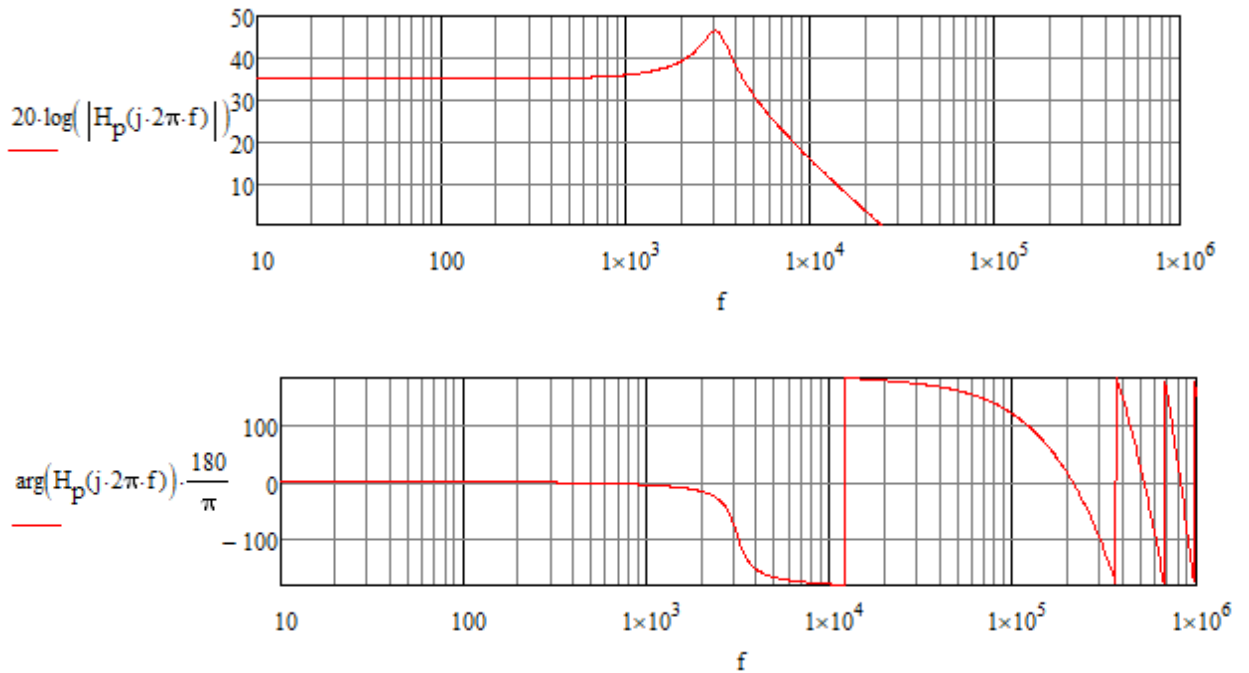


Figure 2-3: VM Plant Gain and Phase based on Nodal Analysis

Modeling Tools for Power Supply Impedance Analysis

Note that the nodal analysis strongly agrees with the SPICE AC analysis. Another important point is that the VM plant has a very sharp negative phase shift due to the output filter. In this case it takes place at 3kHz.

A zero frequency pole (integrator) and two zeros will be used to compensate the loop. Zeros add positive phase shift, therefore the first zero will take place before the output filter resonant point. This is required because there needs to be significant positive phase shift (~ 50 degrees) before the sharp negative phase shift of the filter. Before placing the first zero, be sure to include internal and external load capacitance to determine the output filter resonant point.

The second zero will be placed after the output filter resonant point. One should cancel out the some or all of the external capacitance to determine this frequency selection. A few iterations may need to take place to optimize this selection.

One may wonder, why not put the second zero at an earlier frequency. If the second zero comes too early, the loop will cross zero gain slowly. To achieve gain margin, the gain of the entire loop will need to be lowered. This will have negative effects on dynamic and static load regulation.

For this particular case, zeros are selected to take place at 1500Hz and 5000Hz and the integrator gain is adjusted to cause the loop to cross at 10kHz.

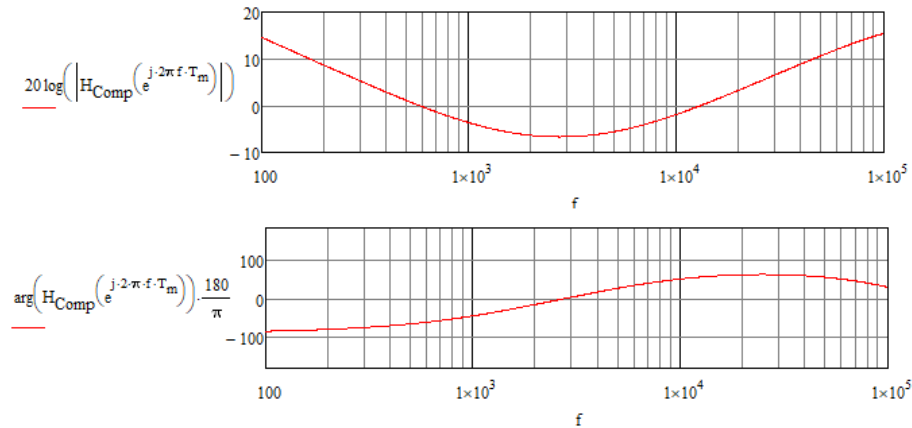


Figure 2-4: VM Compensator

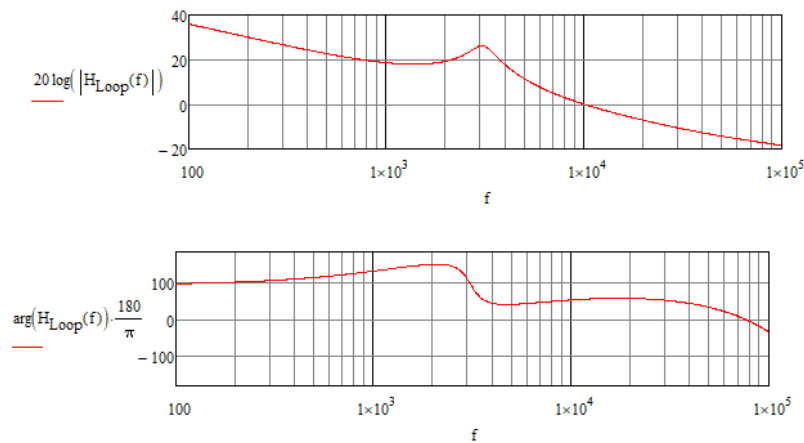


Figure 2-5: VM Complete Loop

Modeling Tools for Power Supply Impedance Analysis

The compensator is now added to the SPICE model in Figure 2-6. E4 acts as a buffer (AKA follower) and E5 acts as an ideal OP Amp.

The integrator gain is set by R6 and C6, the first zero is set by R8 and C6, the second zero is set by C7 and R6.

E6 is an average model of the Sawtooth comparator in a standard VM PWM. It simply translates the output of the Op Amp (E5) into a duty cycle level.

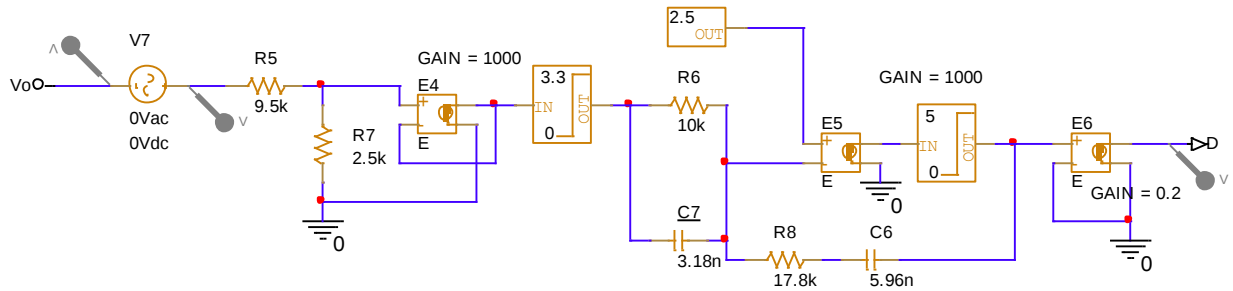


Figure 2-6: VM Compensator in SPICE

Figure 2-7 is a SPICE AC analysis of the complete VM loop. We can see it matches the target calculations from the nodal analysis.

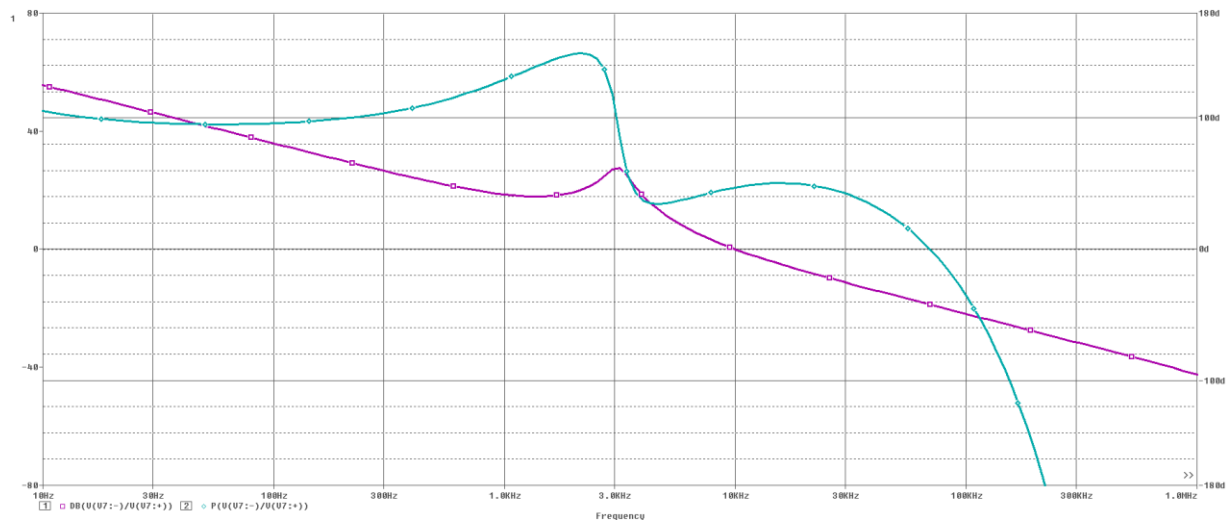


Figure 2-7: Total VM Loop Gain and Phase

2.4 Matching the EMI Filter

An EMI filter is added to the front end of the power supply. The design uses a multistage 4 pole filter with a dampening network incorporated. The filter provides approximately 60db of attenuation at the switching frequency. The dampening network limits the impedance to 1 ohm (0 dbOhm) at the resonant point.

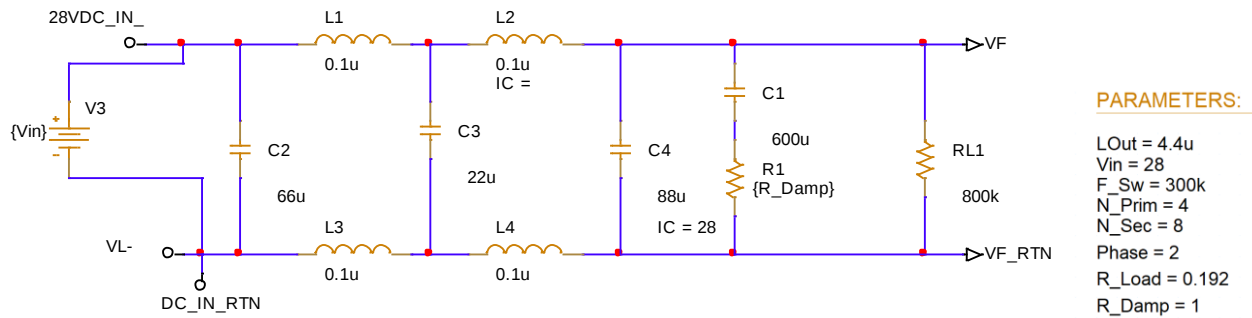


Figure 2-8: EMI Filter Added to SPICE Model

To plot the impedance characteristics we can refer back to Figure 2-1, set source V6 to a modest number, 0.1VAC for example. V8 should be set to zero and V7 should have already been removed as it was replaced by the VM compensator in Figure 2-6.

Current and voltage 'probes' can be placed on each side of V6 to obtain impedance graphs looking forward into the converter and looking backward into the EMI filter.

The post processor can do all of the work.

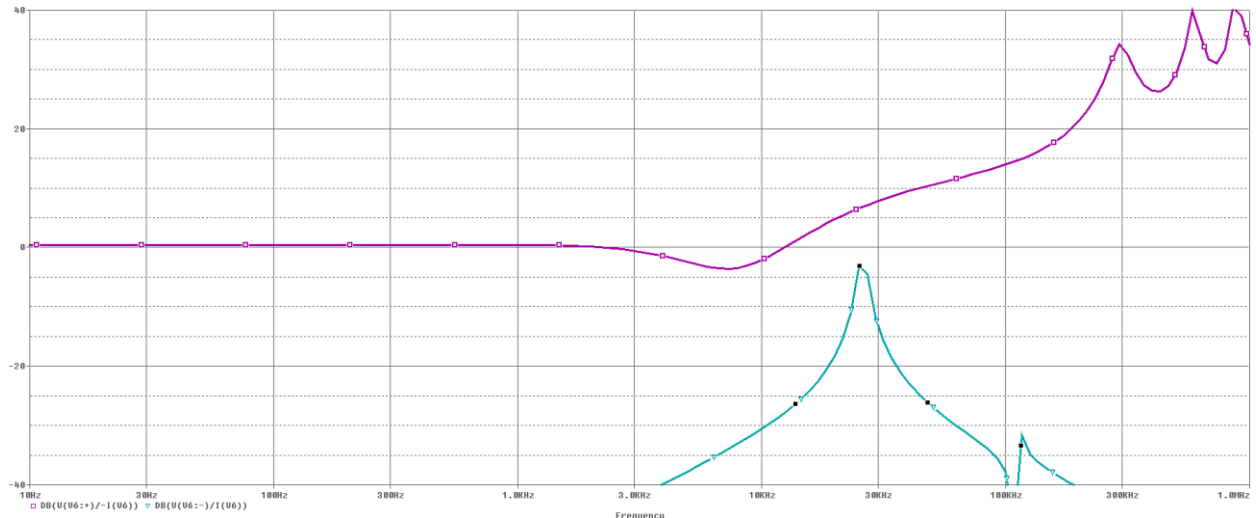


Figure 2-9: VM Impedance Match Plot

2.5 Impedance Margin for the VM Converter

Using the 'parameter' feature within SPICE, we can sweep various parameters to determine if we are satisfied with the results.

As an example, the input voltage will be swept from 18 to 38 volts to examine the effect. This is shown in Figure 2-10.

We see at 18V input, the converter impedance dropped significantly to where the impedance curves are dangerously close. If 18V is a steady state condition, then the margin should be dramatically increased. If it is a transient condition, some minor improvement may be required.

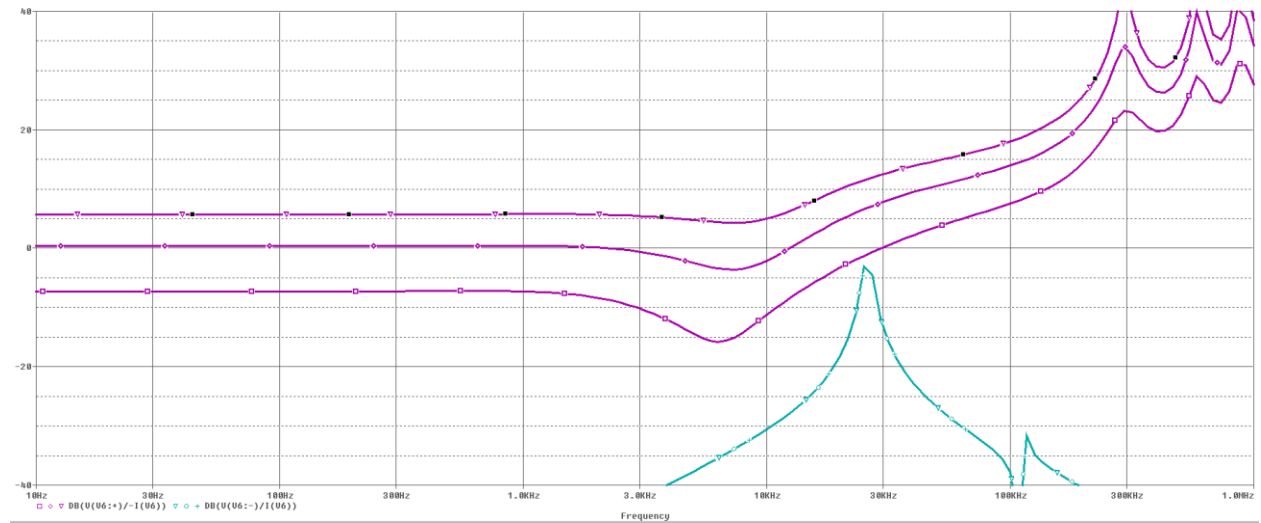


Figure 2-10: VM Input Voltage Variation

3 Average Model for Current Mode Impedance Analysis

Moving along to current mode, we are not going to change a lot, but we need to add a few critical components.

In the voltage mode controller, the output of the controller was divided down linearly to produce a duty cycle. This controller output was proportional to duty cycle.

For current mode, we want the controller output to be proportional to the 'commanded' output current (AKA peak inductor current). Therefore we need an element to turn commanded current (output from the Op Amp) into Duty Cycle (input to the power train).

3.1 Mathematical Representation of Duty Cycle Generator

For buck derived circuits, the inductor current during the DC on time can be represented by

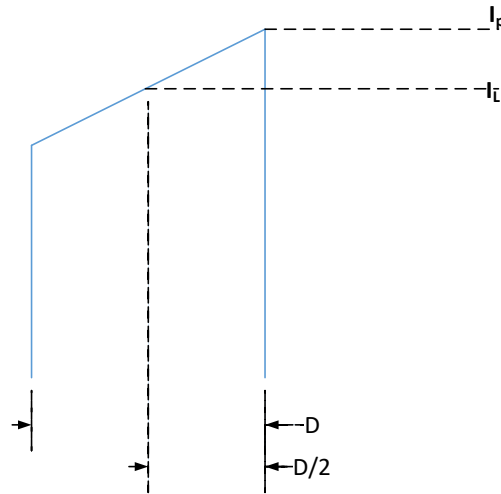


Figure 3-1: VM Input Voltage Variation

The commanded Current from the controller is i_P , The resulting average current is i_L

$$i_P = i_L + \frac{v_L}{L} * \Delta T , \text{ where } \Delta T = \frac{d}{2} * \frac{1}{F_{SW}}$$

Solving for d yields...

$$d = (i_P - i_L) * \frac{2F_{SW}L}{v_L}$$

Equation 3-1: Average DC from Commanded Current

Modeling Tools for Power Supply Impedance Analysis

This is a fairly simple equation, except for one problem... The inductor voltage varies and requires SPICE to perform real-time division. There is no such function in SPICE, so we must introduce a method.

3.2 Emulating Division in PSPICE

Reversing the multiplication process can be approximated using multiplication fed back to a gain stage. If we reverse multiplication in this way, we will get an approximation of division. This approach is shown in Figure 3-2.

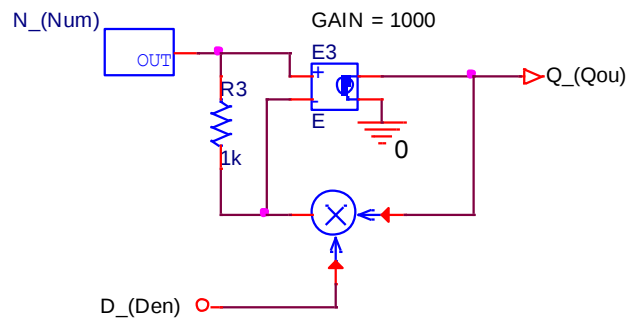


Figure 3-2: Division Emulator

We can examine how this works mathematically, then understand the limits.

Following the schematic, we can write an expression for Q

$$Q = 1000 * (N - (Q * D))$$

We can now expand the equation

$$Q = 1000N - 1000Q * D$$

Gather the Q terms

$$Q(1 + 1000D) = 1000N$$

Finally, solve for Q

$$Q = \frac{1000N}{1 + 1000D}$$

We can see that Q is a pretty good representation of division, as long as $1000D$ is much greater than 1.

In this case, the denominator is the voltage across the inductor, v_L . This will always meet the criterion.

3.4 SPICE Representation of Average CMC Power Train

We can now represent the Power Train (AKA plant) for the Average CMC Model.

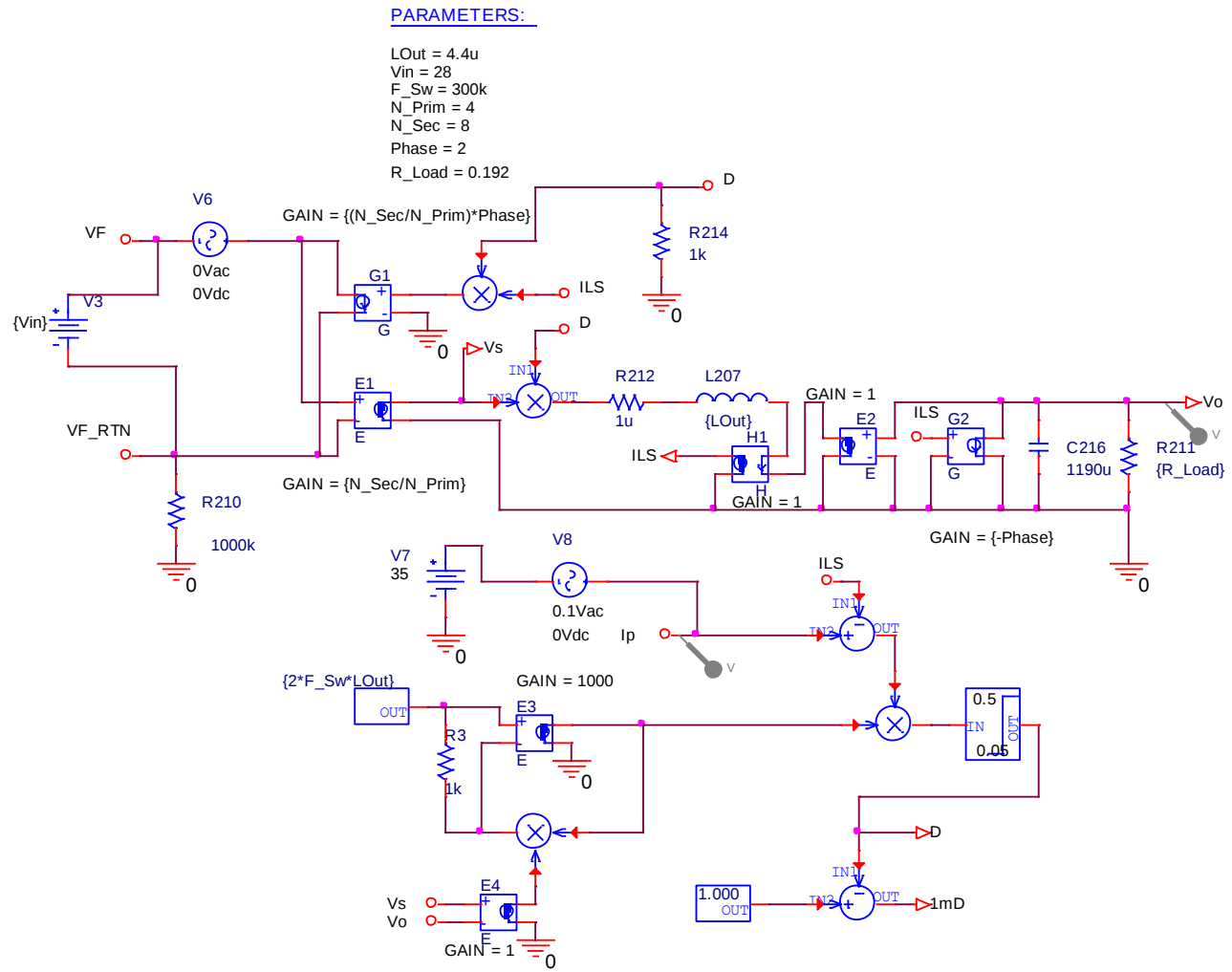


Figure 3-4: CMC Plant Average Model

Here, the input is the Current command at node I_p . I_{LS} is the resulting inductor current in a single output inductor. The parameter 'phase' is set to 2, so the total output current is twice that of an individual inductor. Setting phase to 2 would be used for a current doubler or a two phase topology. It can be set to represent any number of phases used in a buck derived topology.

3.5 CMC Plant Gain

Here, the input is the Current command at node Ip. ILS is the resulting inductor current in a single output inductor. The parameter 'phase' is set to 2, so the total output current is twice that of an individual inductor. This setting would be used for a current doubler or a two phase topology.

An AC sweep can be used to determine the Gain of the CMC Plant. Some Critical points will be logged.

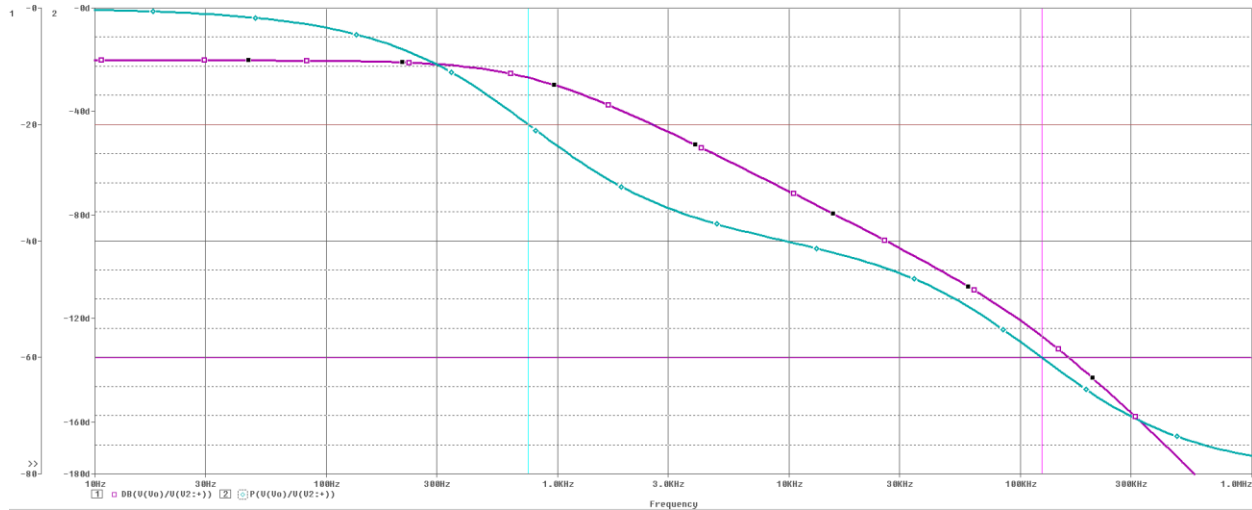


Figure 3-5: CM Plant Gain and Phase

The sweep shows some expected results. There is flat gain at low frequency. This is the programmed current times the load resistor. Then there is a dominant pole at 750 Hz. This is where the output capacitor becomes dominant over the load resistor. Then there is another pole at about 125kHz, this is where the current mode control process breaks down.

The 90° phase shift point occurs at 10kHz. We would like to cross before this point because the phase drops off more rapidly after this point. Other considerations are component variances and external load characteristics added at the next level of use. We're going to set the target crossover frequency to that 10 kHz. If higher load transient performance is required, the crossover frequency goal can be increased. This model can be tested for load transient performance. It would be best to include parasitic resistances such the ESR of the output capacitor to get the best representation.

At 10 KHz, the plant gain is -31.5 db and the phase is -90°.

3.6 Control Loop and Compensation

We are now ready to add the control loop section to the project. The error amplifier will be represented by an ideal gain stage where the input is the error of programmed voltage to feedback voltage. The current sense is represented by a gain of 20 x. This equates to 5V from the error amplifier representing 100A of programmed current per inductor. The controller is shown at the bottom of Figure 3-6.

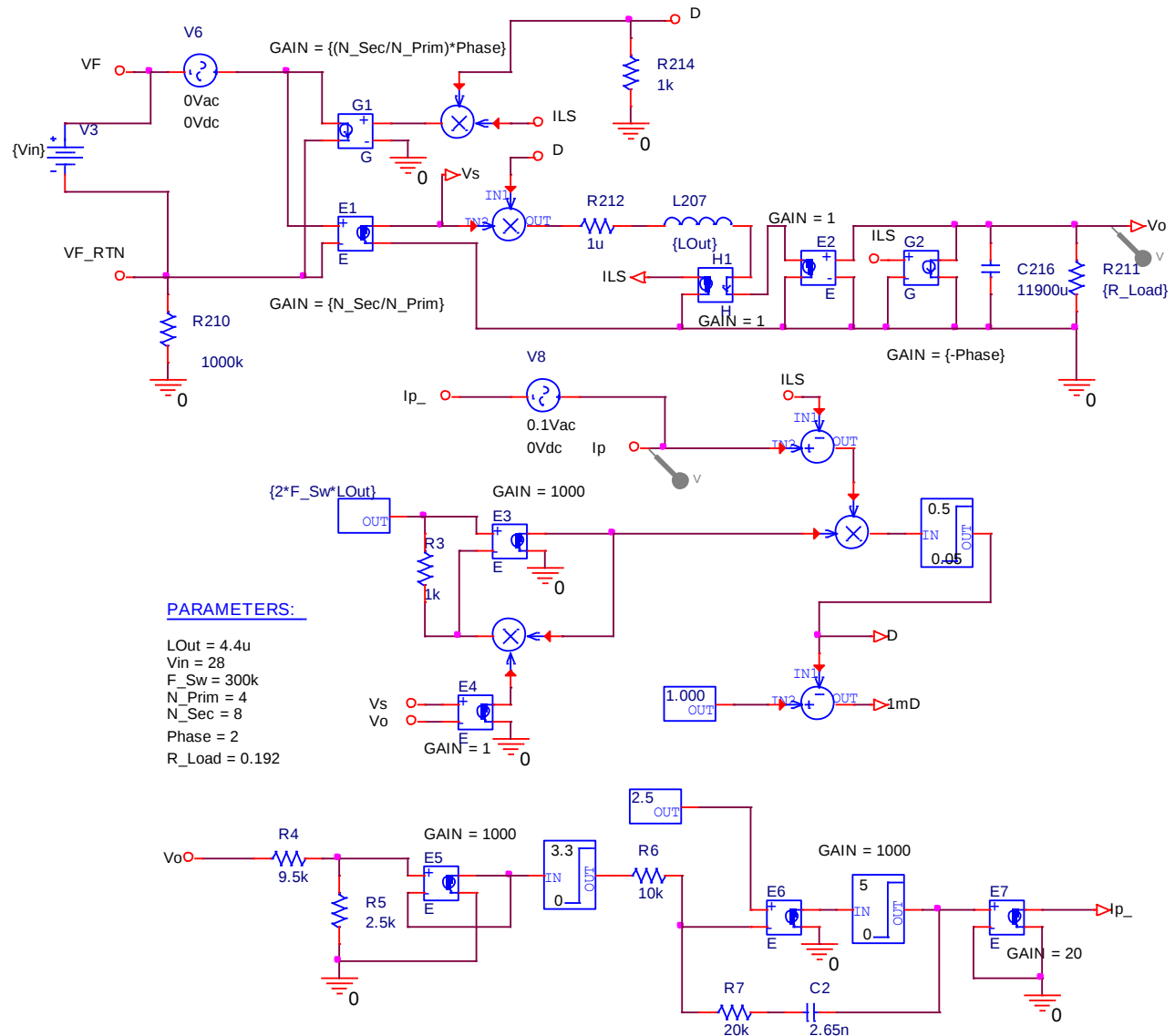


Figure 3-6: CMC with Voltage Controller

Modeling Tools for Power Supply Impedance Analysis

The voltage sense has a gain of 2.5 : 12 or -13.6db, the current sense has a gain of 20 or 26db. Previously, we saw the gain of the plant is -31.5 db at the 10 kHz desired crossover. We want the total gain to be unity at the crossover.

$$G_{Comp_{10kHz}} = -(G_v + G_{cs} + G_{Plant_{10kHz}})$$

$$G_{Comp_{3kHz}} = -(-13.6db + 26db + -31.5db) = 19.1 db = 9.02 X$$

$$R_{Comp} = G_{Comp_{10kHz}} * 0.707 * R_{FB}$$

$$R_{Comp} = 9.02 * 0.707 * 10k = 63.7k$$

$$C_{Comp} = \frac{1}{2\pi * F_{SW} * R_{Comp}}$$

$$C_{Comp} = \frac{1}{2\pi * 10 kHz * 63.7k} = 250 pF$$

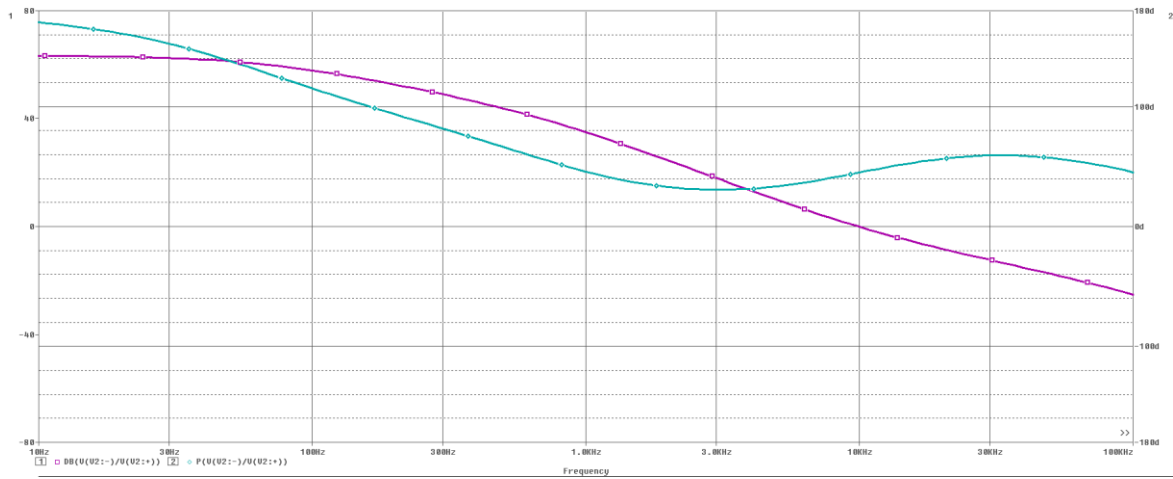
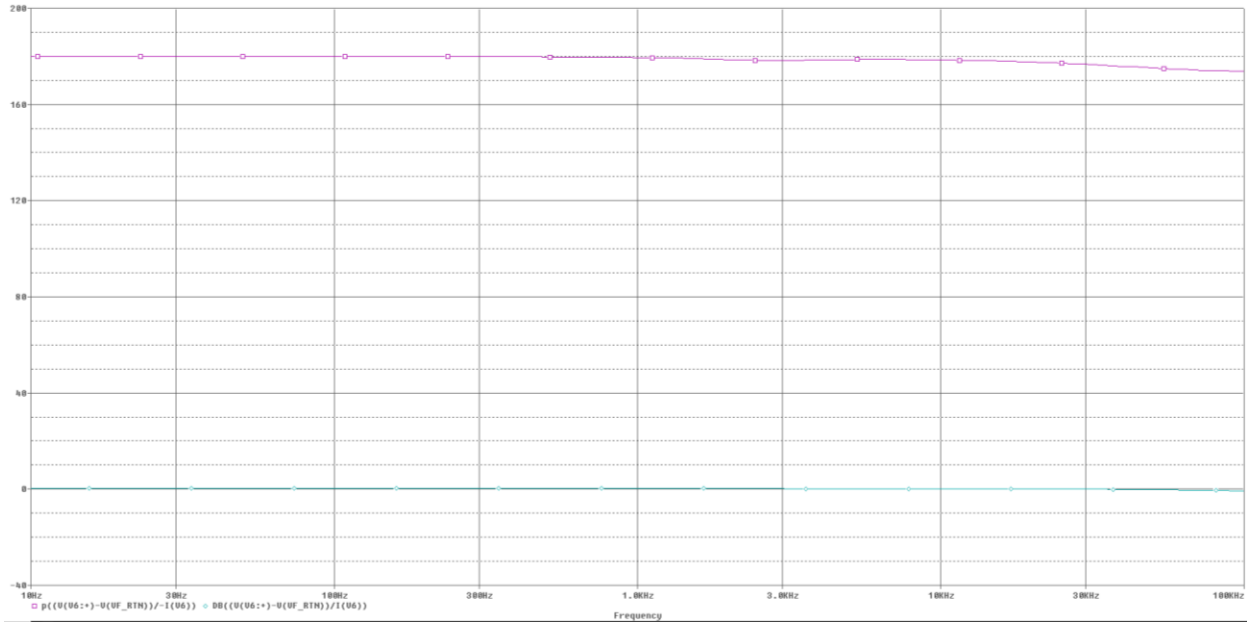


Figure 3-7: CMC Open Loop Response

The calculations achieved unity gain at 10 kHz with 57 degrees of margin.

3.7 Input Impedance Plot

An input impedance plot can now be taken from the simulation. This is done by performing an AC Sweep, but changing the insertion point to the input. We can then measure input current and voltage to arrive at the input impedance.



With a CMC we are getting a relatively flat line. In this case the input impedance is about an ohm, which makes sense for this application. Note that the phase of the impedance is at 180 degrees. This is because the converter appears as a constant power element at its input. When voltage increases, current decreases. From an AC standpoint, the current is out of phase with the input voltage. This characteristic has been called a negative input impedance.

3.8 CMC Input Impedance Plot

We now try to attach the same EMI filter. We find that we lost margin.

This is because our EMI filter peaks at 30kHz to -2.5 dbΩ. At this frequency, the impedance of the VM circuit is determined by the output inductor reflected through the transformer. The impedance at this frequency is about 8 dbΩ higher than the low frequency impedance of 0dbΩ. The total difference is 10.5 dbΩ.

Since the CMC has high frequency pulse by pulse current regulation, the current control loop remains at 30 kHz to shield us from the output inductor. The load impedance remains at 0 dbΩ.

This reduced the margin to 2.5 dbΩ.

The remedy at this point is to reduce the dampening resistor to 0.5 dbΩ to restore the margin.

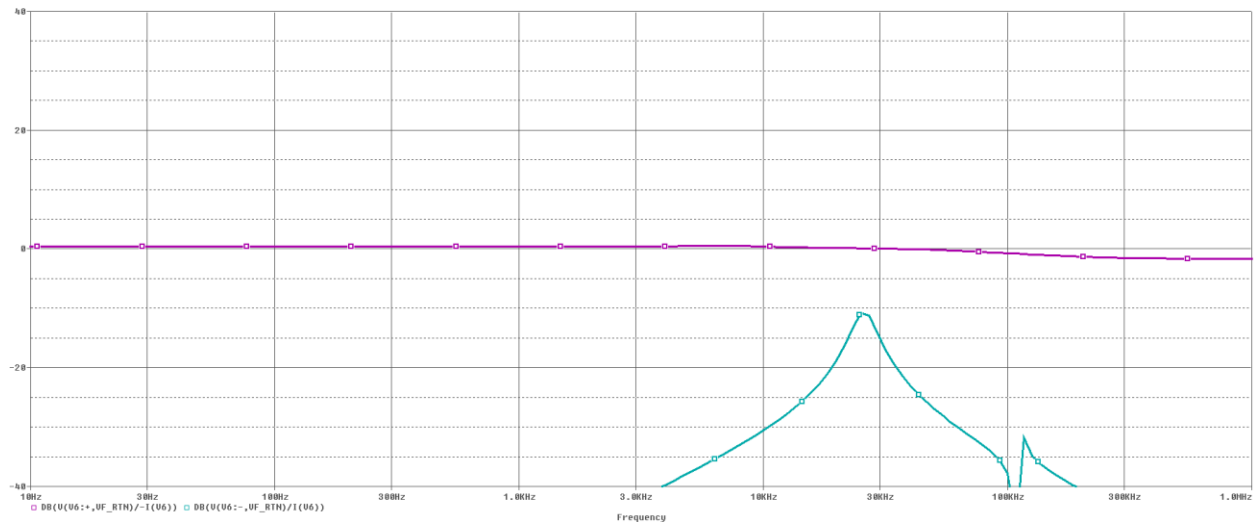


Figure 3-8: CMC Impedance Match Margin Restored

4 Effect of adding Line Impedance Stabilization Networks (LISN)

LISN networks are introduced by several different test standards. Their purpose is twofold. One is to provide a standard observation point for conducted emissions. The second is to harmonize the expected input line impedance across a highly diverse world of suppliers.

Up to this point, we analyzed circuits with perfect power sources that have 0Ω impedance.

When a test engineer shows up with a LISN in hand to verify product performance, we should already have confidence that oscillation due to an impedance mismatch will not occur.

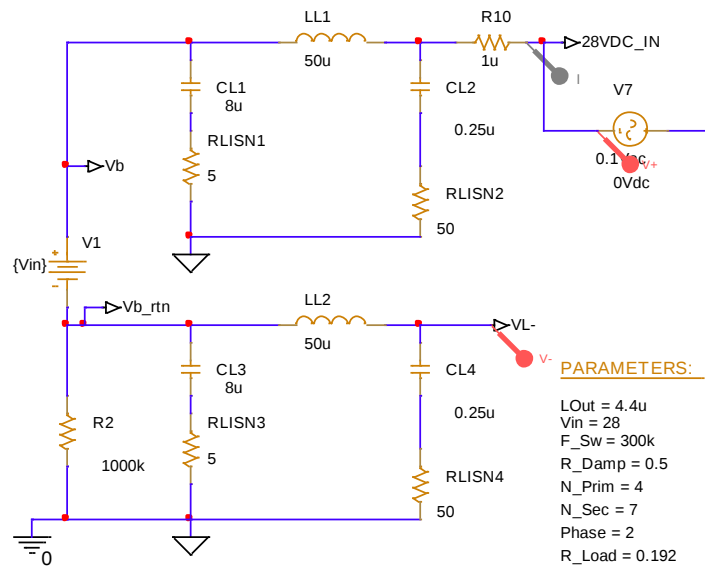


Figure 4-1: Typical LISN from MIL-STD-461

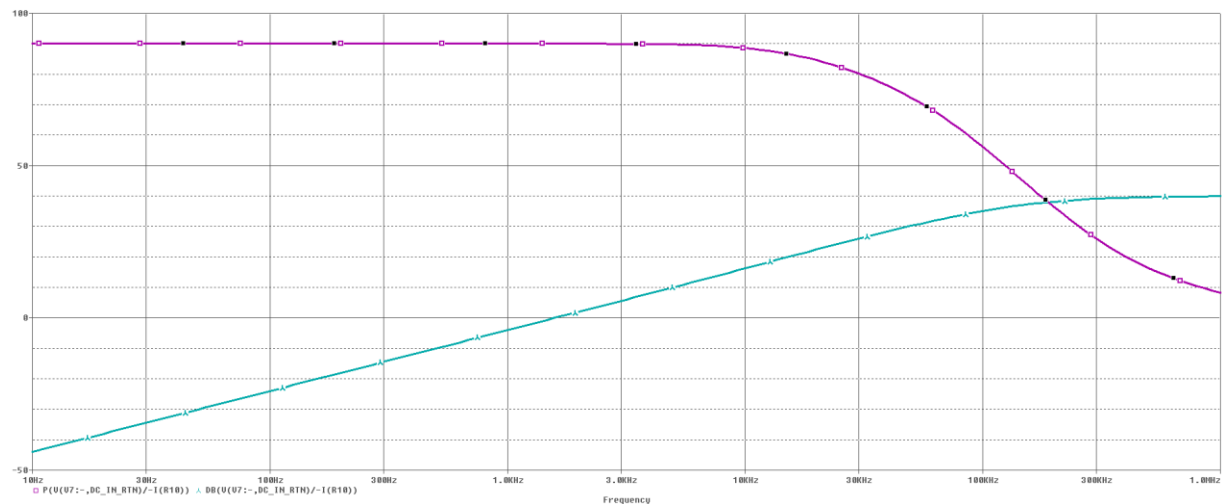


Figure 4-2: LISN Impedance Curve

Modeling Tools for Power Supply Impedance Analysis

We can see that the LISN impedance crosses the 0 dbΩ point at 1.59 kHz. More than likely, this will represent a problem once connected.

The LISN is added to the model in place of the ideal source. Impedance match will be re-evaluated.

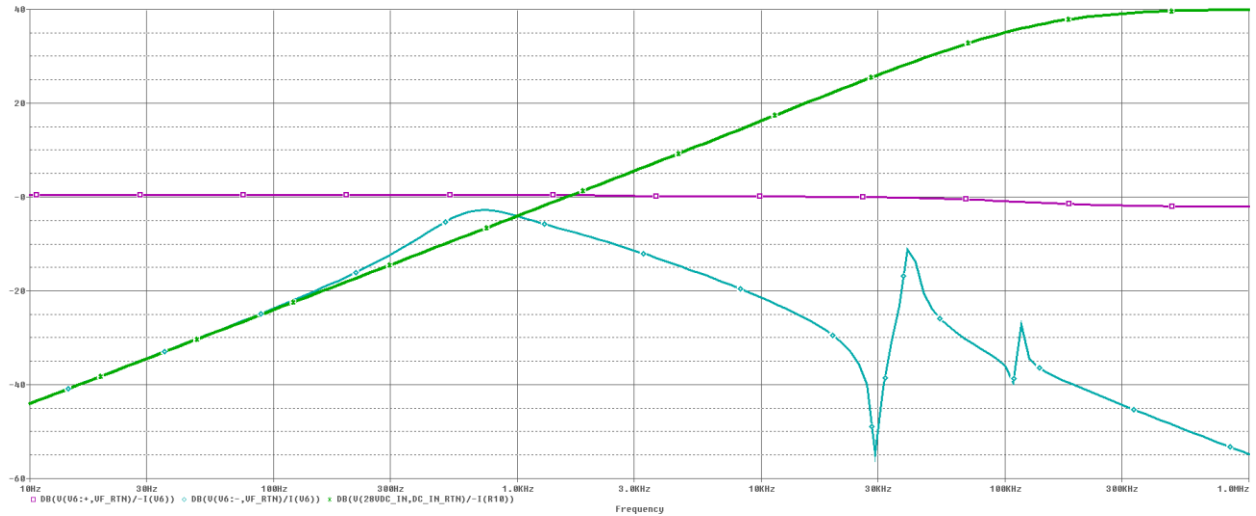


Figure 4-3: Impedance Match with LISN Connected

NOTE : The green trace on the figure is the LISN impedance shown for reference.

We can see our original peak at 30 kHz due to the EMI filter, but now there is a new low frequency peak at about 800Hz. This reduces the margin to less than 3dbΩ.

The LISN has become the Dominant Limiting Design Factor. We must now re-engineer our dampening network in order to work with the LISN.

Target LF Resonance to occur where LISN is 15db Lower than the converter. 300Hz.

The extra 5 db allows for some level of Q Factor.

Calculate Dampening Resistor to Provide 10db Margin. $R_D = -10\text{db}\Omega * 0.707 = 0.22\Omega$

Calculate Dampening Cap to Resonate at 300Hz. $C_D = \frac{1}{2\pi f X_C} = \frac{1}{2\pi * 300 * 0.22} = 2400\mu F$

Modeling Tools for Power Supply Impedance Analysis

The updated impedance plot is now evaluated.

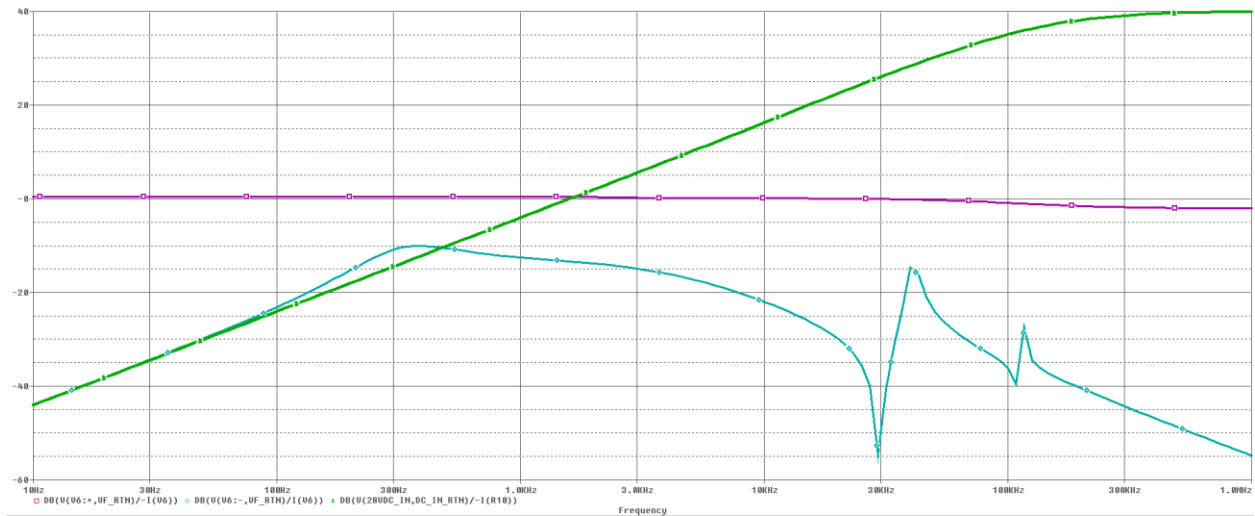


Figure 4-4: Impedance Margin Restored

The 10 db Margin is restored, however the cost is significant.

The dampening capacitor went from 600uF to 2400uF while the resistor is reduced to 0.22 ohms. The volume for the capacitor may be four times larger. The resistor size will also increase because it will dissipate more power when exposed to susceptibility environments.

This level of margin may be considered to be too conservative, but we must also remember that we will lose about 6 db of margin if the input line varies down to 18V.

5 Effect of Using Transient Voltage Test Equipment

Most single quadrant power sources are designed to have low source impedance. This is done to allow these sources to be used as general purpose equipment for the masses. These sources are not generally used for rapid rise times or transitions.

Four quadrant transient voltage testers are quite different. They cannot approach the low impedances of their counter parts because they must support rapid rise and fall times. What makes matters worse, these sources are designed for multi-purpose. The same source that is designed to provide 28VDC is also expected to provide 270VDC as well as 115VAC up to 400Hz and beyond.

The end result is that a high power transient source may have difficulty driving a modest low voltage power supply.

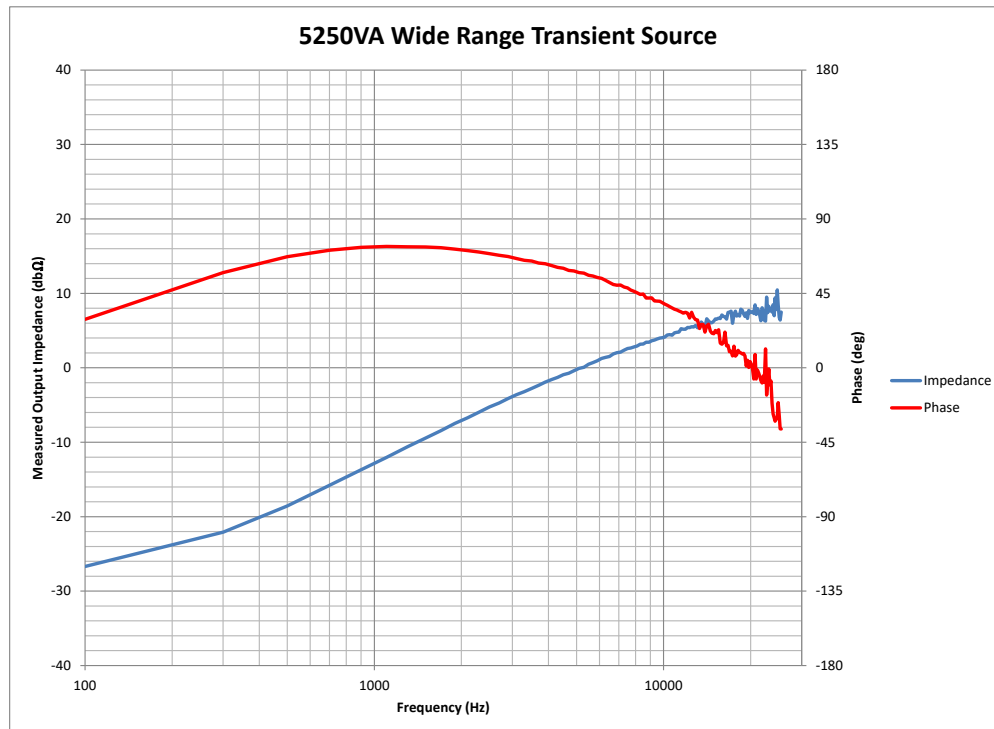
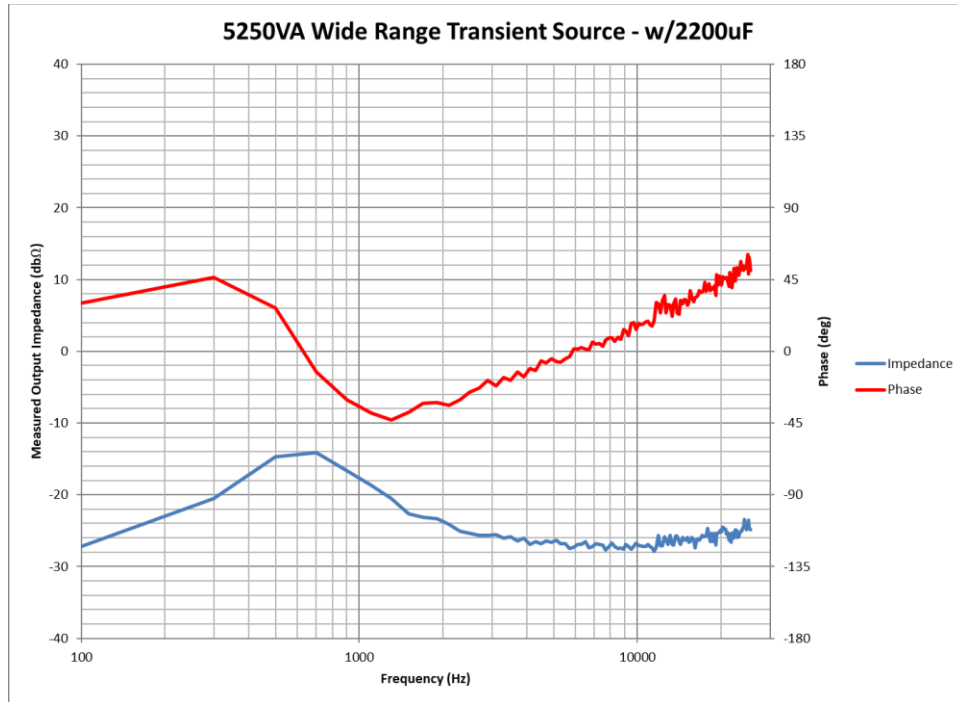


Figure 5-1: Measured Output Impedance of Transient Power Source

A Source rated for 5250 Watts reaches 0 dbΩ at 5 kHz and violates the 10 db margin at 1.5 kHz. This source would have difficulty powering a 750W 28V Power supply.

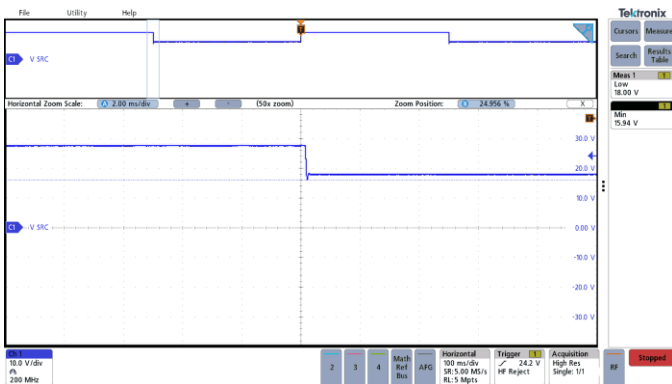
Modeling Tools for Power Supply Impedance Analysis

One solution would be to a bulk capacitor to the output of the power source. This lowers its impedance dramatically.

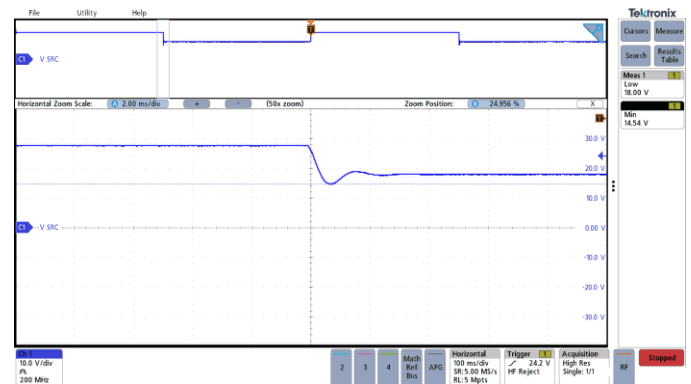


With 2400uF added to the source, the impedance is lowered to less than -14 dbΩ.

The problem with this addition, we have made the source less stable, increased the overshooting, and slowed down the slew rate. The capacitor is also being stressed.



5250VA Transient Generator 5A load No Capacitor



2200 uF Capacitor added to Output of Source

Modeling Tools for Power Supply Impedance Analysis

The solution is to compromise. Instead of adding a Capacitor, add a dampening network, Using a 2200 uF capacitor with a 0.33Ω resistor in series reduces the source impedance to -10dbΩ. This minimizes the impact on slew rate, eliminates overshoot and undershoot and reduces stress on the added capacitor.



Figure 5-2: Improved Transient Performance with Dampener

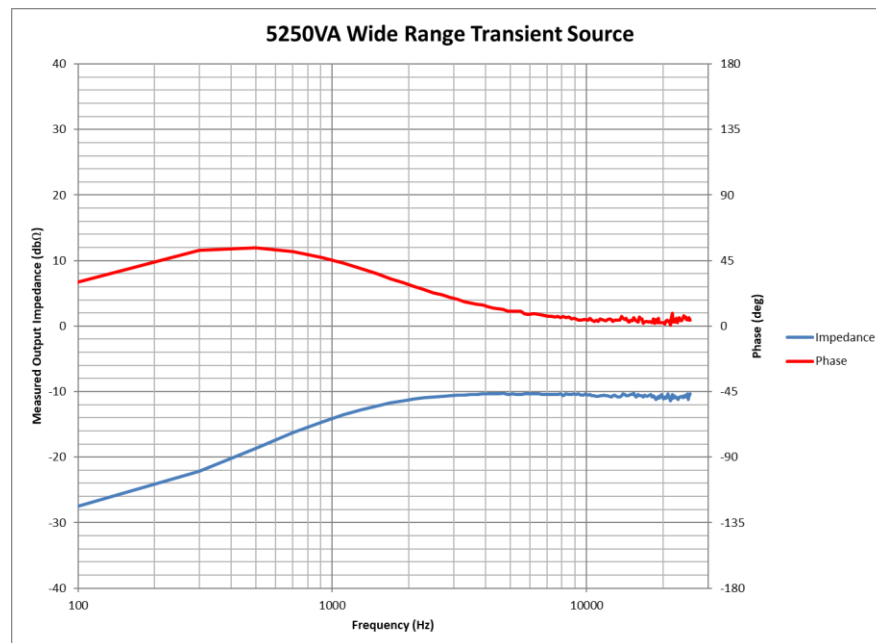


Figure 5-3: Transient Source Impedance with Dampener Added